64 POINT 8-BIT FAST FOURIER TRANSFORM

ZACK FRAVEL

WHAT IS AN FFT?

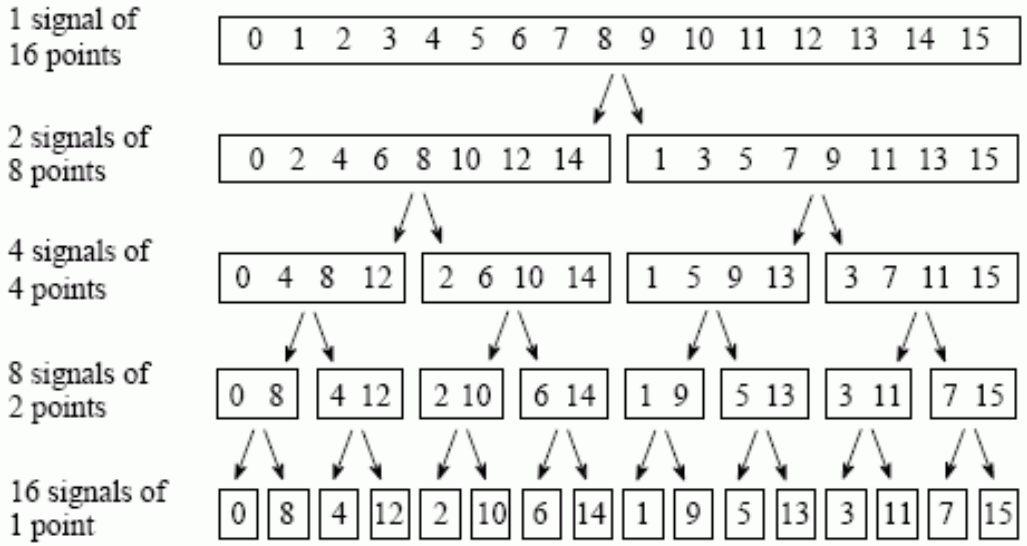


FIGURE 12-2
The FFT decomposition. An N point signal is decomposed into N signals each containing a single point. Each stage uses an *interlace decomposition*, separating the even and odd numbered samples.

http://www.dspguide.com/graphics/F_12_2.gif

- Algorithm that allows analysis through time and frequency translation
- Complex numbers describe information in the time and frequency domains

REAL WORLD APPLICATIONS

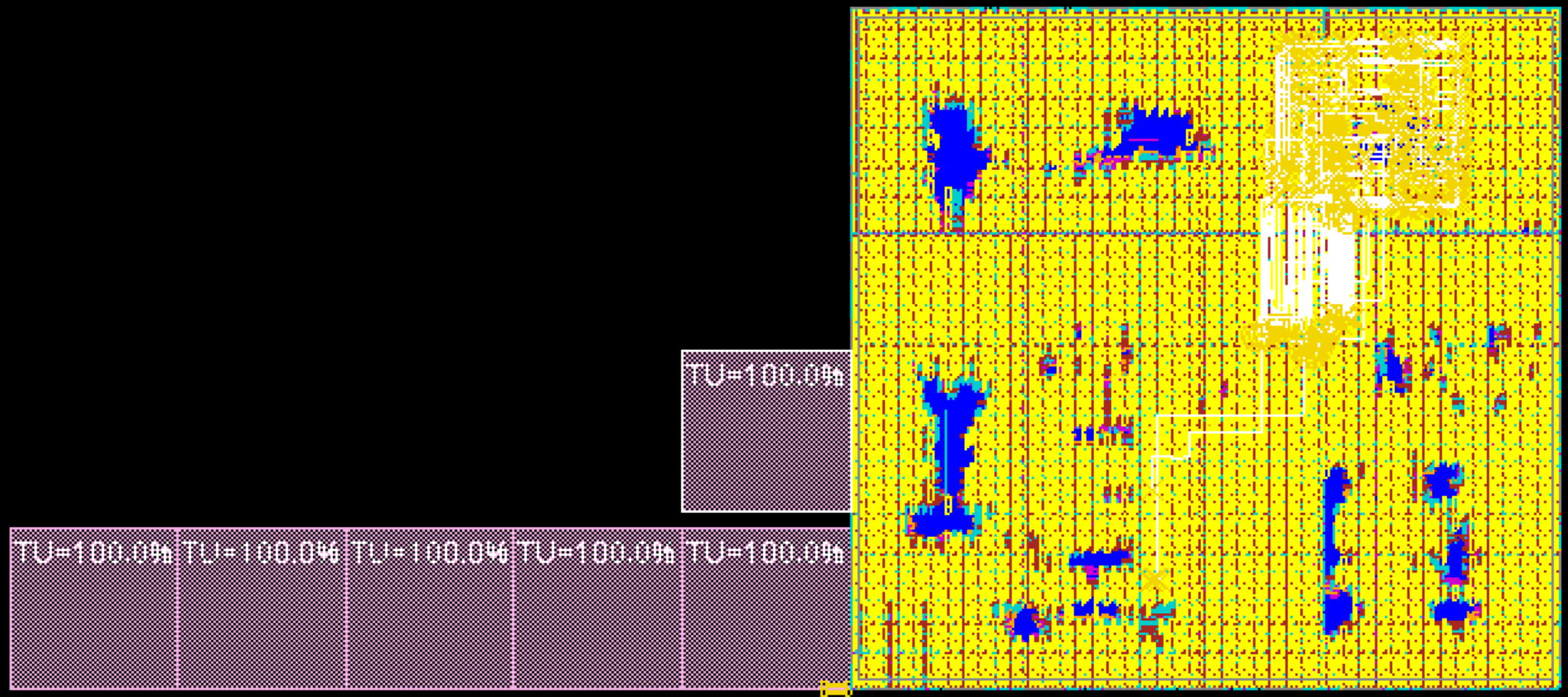
- Imaging Analysis
- Telecommunications
- Automotive
- Countless applications in digital signal processing (DSP)
- Why not perform digitally?
  - Real-time applications
  - Speed (Dedicated logic allows continuous real-time operation)

DESIGN OVERVIEW

- 20 multipliers (8x8)
- 34 adders (8x8)
- 6 RAMs (64 words, 16 bits per word)

HOW IT WORKS

- Throughput: 1 transform every 32 cycles
- 18 stages
- Uses an interleaved complex data format
  - X[0] points to the real component
  - X[1] begins the imaginary component
- System requires a 32 cycle gap between input vectors
- Flag signals for indicating data stream (next, next_out)
- Circuit has a latency of 145 cycles
  - next_out asserted 145 cycles after next


TU=100.0%
TU=100.0%
TU=100.0%
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TU=100.0%
TU=100.0%

SYNTHESIS

- Synopsys Design Compiler
- Nangate Open Cell Library

- 40ns clock cycle
- 25 MHz
- RTL provided with full functionality
- Generates gate-level netlist to be used in placement and routing

```
set_host_options -max_cores 6

set_app_var link_library "/home/zpfravel/Desktop/fft8_nangate/lib/db/NangateOpenCellLibrary_typical_ecsm.db"
set_app_var target_library "/home/zpfravel/Desktop/fft8_nangate/lib/db/NangateOpenCellLibrary_typical_ecsm.db"
set_app_var symbol_library "generic.sdb"

define_design_lib work -path ./work

set topname fft8
set verilogs [glob $topname.v]

set myPeriod_ns 40
set myClk clk

analyze -format verilog  $verilogs

elaborate $topname

current_design $topname

link

create_clock -period $myPeriod_ns $myClk

compile_ultra

redirect $topname.timing.dc.rpt {report_timing}
redirect $topname.area.dc.rpt {report_area}
redirect $topname.power.dc.rpt {report_power}

write_sdc $topname.sdc
write -format verilog -hierarchy -output $topname.syn.v

quit
```

DESIGN COMPILER SCRIPT (DC.TCL)

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : fft8
Version: M-2016.12-SP5
Date   : Mon Dec  4 00:00:19 2017
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

  Startpoint: stage9/codeBlockIsnt16714/tm41_reg[1]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: stage9/codeBlockIsnt16714/m14983/q_reg[0][15]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  fft8               5K_hvratio_1_1        NangateOpenCellLibrary

  Point                                                   Incr       Path
  ------------------------------------------------------------------------
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  stage9/codeBlockIsnt16714/tm41_reg[1]/CK (DFF_X1)       0.00 #     0.00 r
  stage9/codeBlockIsnt16714/tm41_reg[1]/QN (DFF_X1)       0.16       0.16 r
  U11050/ZN (NAND2_X1)                                    0.06       0.22 f
  U11051/ZN (OAI21_X1)                                    0.08       0.30 r
  U11052/ZN (INV_X1)                                      0.09       0.39 f
  U11056/ZN (AOI21_X1)                                    0.16       0.55 r
  U11087/ZN (INV_X1)                                      0.06       0.61 f
  U11088/ZN (OAI22_X1)                                    0.08       0.69 r
  U11089/Z (XOR2_X1)                                      0.09       0.78 r
  U11090/ZN (OAI22_X1)                                    0.05       0.83 f
  U11091/ZN (AOI21_X1)                                    0.06       0.89 r
  U11092/ZN (AOI21_X1)                                    0.03       0.92 f
  U11098/ZN (OAI21_X1)                                    0.05       0.97 r
  U11103/ZN (AOI222_X1)                                   0.05       1.02 f
  intadd_1/U8/CO (FA_X1)                                  0.11       1.13 f
  intadd_1/U7/CO (FA_X1)                                  0.09       1.22 f
  intadd_1/U6/CO (FA_X1)                                  0.09       1.31 f
  intadd_1/U5/CO (FA_X1)                                  0.09       1.40 f
  intadd_1/U4/CO (FA_X1)                                  0.09       1.49 f
  intadd_1/U3/CO (FA_X1)                                  0.09       1.58 f
  intadd_1/U2/CO (FA_X1)                                  0.09       1.67 f
  U11166/ZN (OAI21_X1)                                    0.05       1.72 r
  U11167/ZN (OAI21_X1)                                    0.03       1.75 f
  stage9/codeBlockIsnt16714/m14983/q_reg[0][15]/D (DFF_X1)
                                                          0.01       1.76 f
  data arrival time                                                  1.76

  clock clk (rise edge)                                  40.00      40.00
  clock network delay (ideal)                             0.00      40.00
  stage9/codeBlockIsnt16714/m14983/q_reg[0][15]/CK (DFF_X1)
                                                          0.00      40.00 r
  library setup time                                     -0.04      39.96
  data required time                                                39.96
  ------------------------------------------------------------------------
  data required time                                                39.96
  data arrival time                                                 -1.76
  ------------------------------------------------------------------------
  slack (MET)                                                       38.19
```

DESIGN COMPILER TIMING REPORT

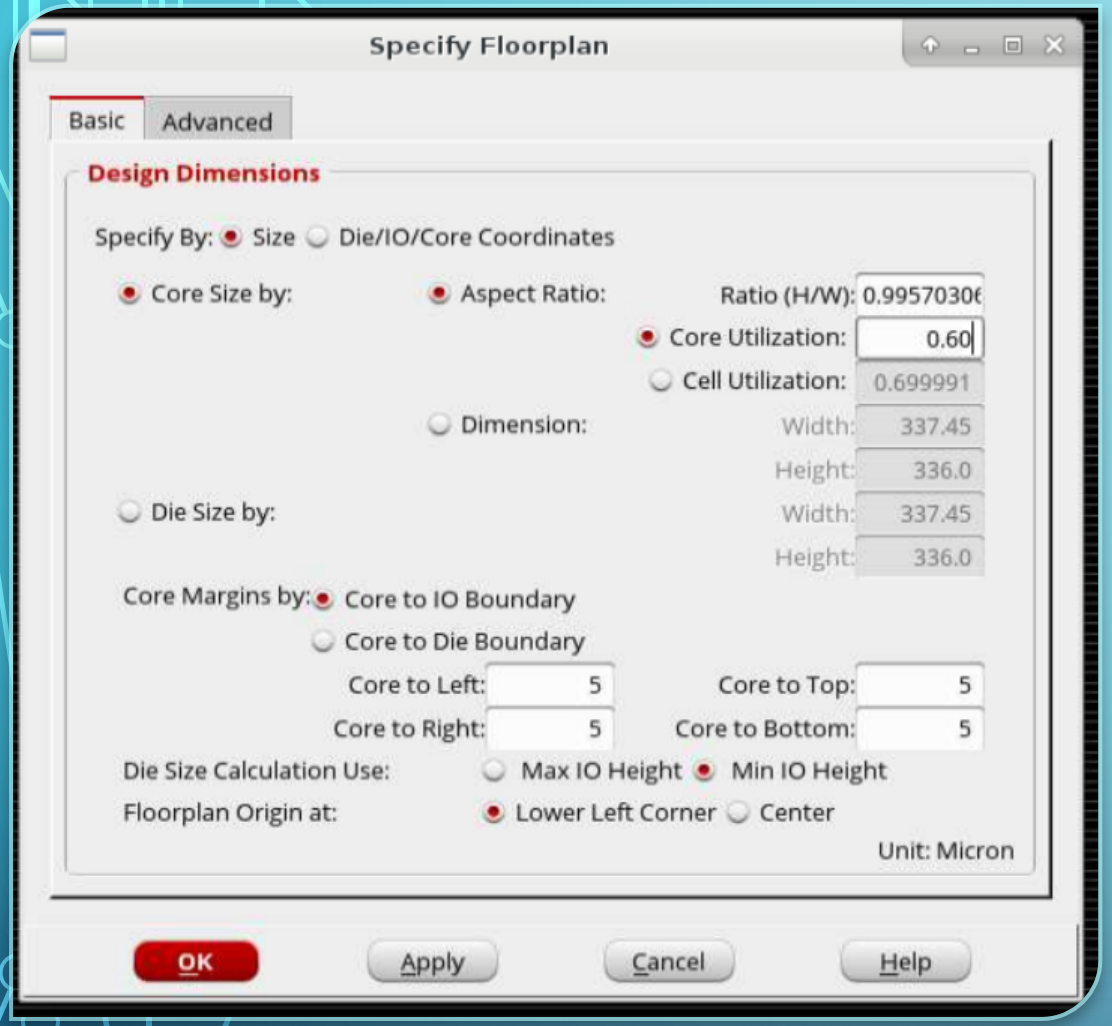
```
****************************************
Report : power
        -analysis_effort low
Design : fft8
Version: M-2016.12-SP5
Date   : Mon Dec  4 00:00:19 2017
****************************************


Library(s) Used:

    NangateOpenCellLibrary (File: /home/zpfravel/Desktop/fft8_nangate/lib/db/NangateOpenCellLibrary_typical_ecsm.db)


Operating Conditions: typical   Library: NangateOpenCellLibrary
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
fft8                   5K_hvratio_1_1    NangateOpenCellLibrary


Global Operating Voltage = 1.1
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V
    Leakage Power Units = 1nW
```

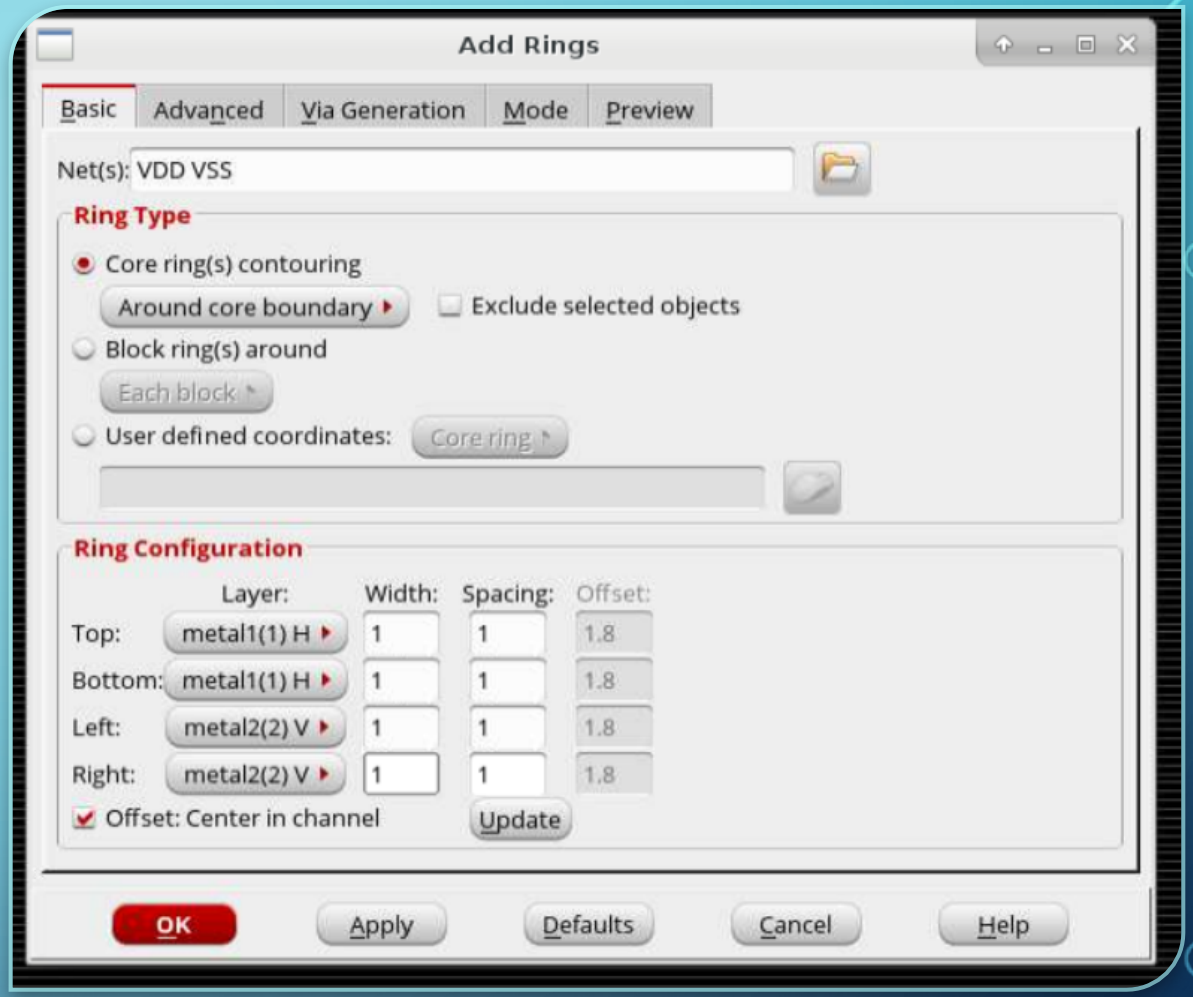
```
  Cell Internal Power  =   1.6745 mW   (94%)
  Net Switching Power  = 107.1543 uW    (6%)
                         ---------
Total Dynamic Power    =   1.7817 mW  (100%)

Cell Leakage Power     =   1.4458 mW


                 Internal         Switching           Leakage             Total
Power Group      Power            Power               Power               Power   (   %    )  Attrs
------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000              0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000              0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000              0.0000  (   0.00%)
clock_network      0.0000           0.0000              0.0000              0.0000  (   0.00%)
register       1.6314e+03          20.8659          8.3070e+05          2.4830e+03  (  76.93%)
sequential         0.0000           0.0000              0.0000              0.0000  (   0.00%)
combinational     43.0769          86.2857          6.1505e+05            744.4151  (  23.07%)
------------------------------------------------------------------------------------------------
Total          1.6745e+03 uW       107.1517 uW      1.4458e+06 nW       3.2274e+03 uW
1
```

DESIGN COMPILER POWER REPORT

PLACEMENT AND ROUTING

- Cadence Innovus Implementation System
- Nangate Open Cell Library
- Optimization performed after both placement and routing steps



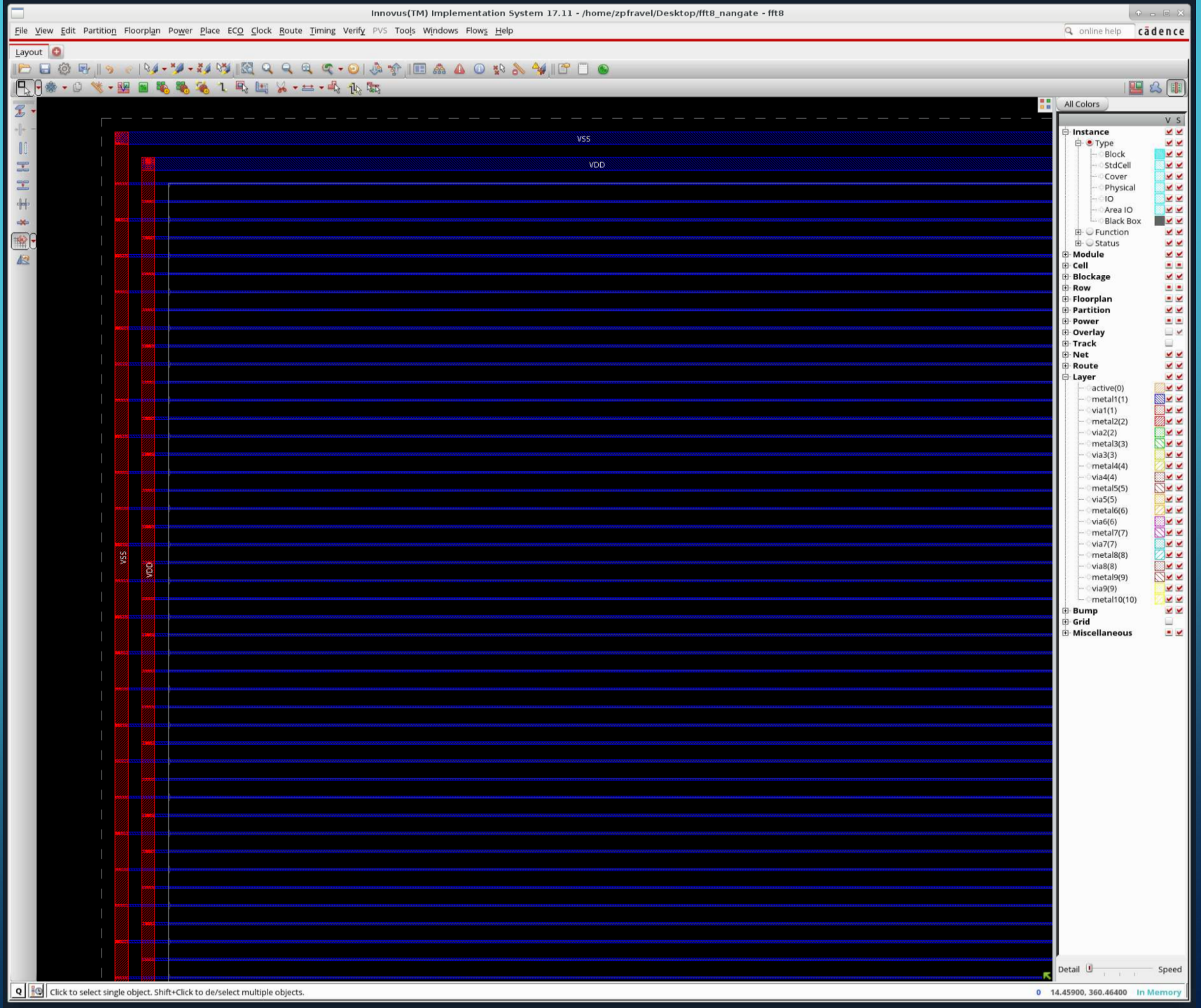


FLOORPLAN AND POWER SETTINGS

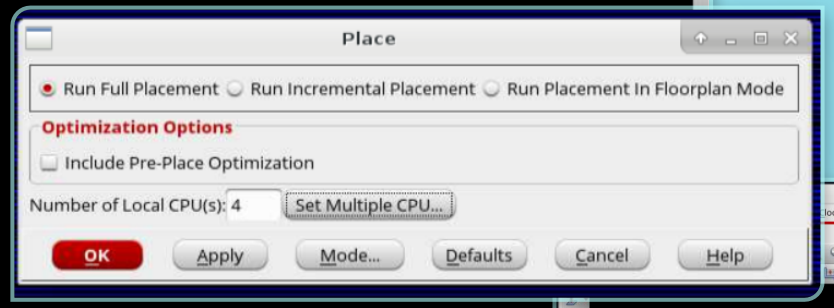
```
 Begin updating DB with routing results ...
 Updating DB with 0 via definition ...Extracting standard cell pins and blockage ......
Pin and blockage extraction finished

sroute created 780 wires.
ViaGen created 520 vias, deleted 0 via to avoid violation.
+--------+----------------+----------------+
|  Layer |     Created    |     Deleted    |
+--------+----------------+----------------+
| metal1 |       780      |       NA       |
|  via1  |       520      |        0       |
+--------+----------------+----------------+
```

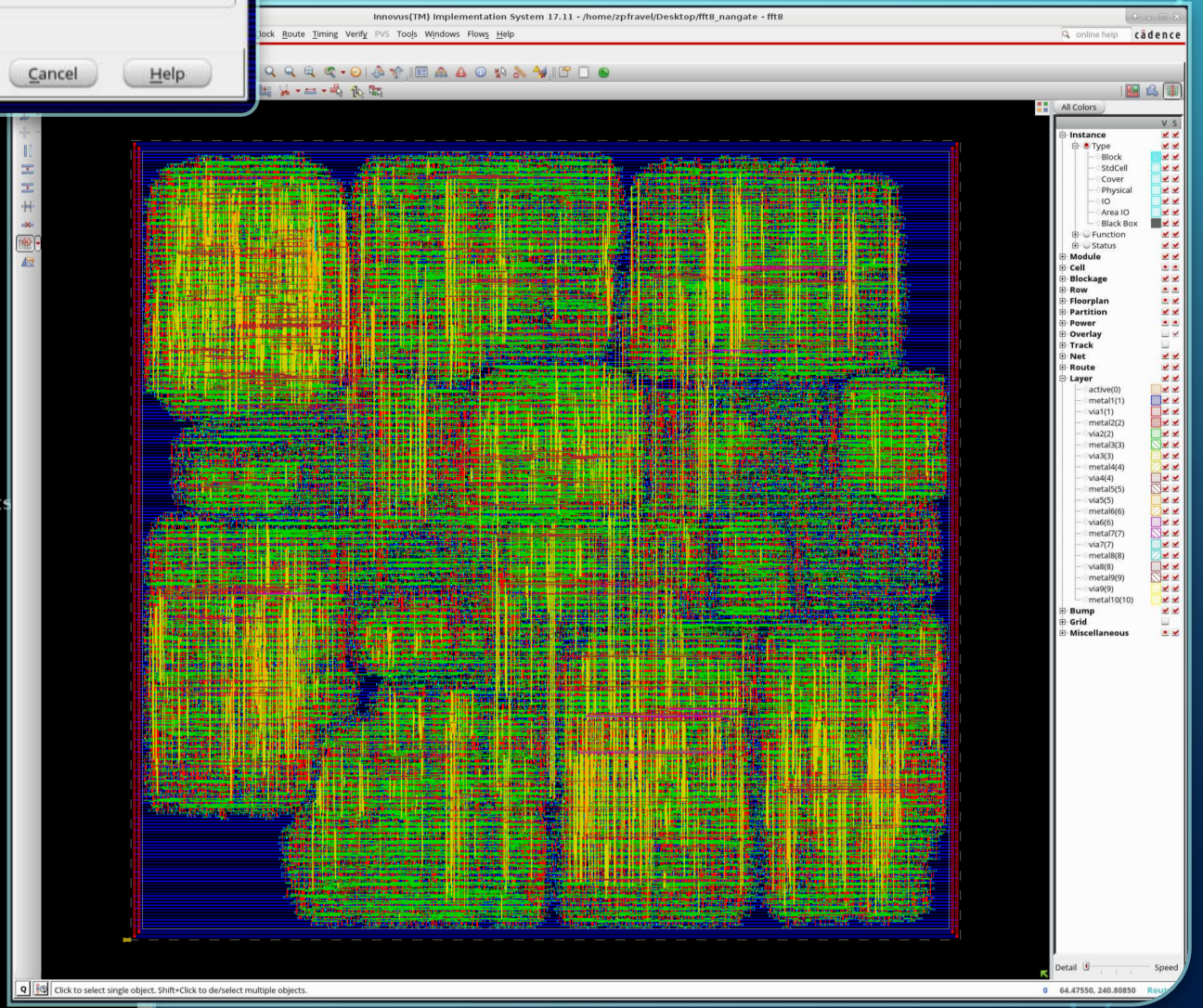
```
innovus 2> The ring targets are set to core/block ring wires.
addRing command will consider rows while creating rings.
addRing command will disallow rings to go over rows.
addRing command will ignore shorts while creating rings.

Ring generation is complete.
vias are now being generated.
addRing created 8 wires.
ViaGen created 8 vias, deleted 0 via to avoid violation.
+--------+----------------+----------------+
|  Layer |     Created    |     Deleted    |
+--------+----------------+----------------+
| metal1 |        4       |       NA       |
|  via1  |        8       |        0       |
| metal2 |        4       |       NA       |
+--------+----------------+----------------+
innovus 2>
```

POWER NETWORK SUMMARY


Innovus(TM) Implementation System 17.11 - /home/zpfravel/Desktop/fft8_nangate - fft8
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help
online help
cadence
Layout
All Colors
VSS
VDD
Instance
Type
Block
StdCell
Cover
Physical
IO
Area IO
Black Box
Function
Status
Module
Cell
Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Net
Route
Layer
active(0)
metal1(1)
via1(1)
metal2(2)
via2(2)
metal3(3)
via3(3)
metal4(4)
via4(4)
metal5(5)
via5(5)
metal6(6)
via6(6)
metal7(7)
via7(7)
metal8(8)
via8(8)
metal9(9)
via9(9)
metal10(10)
Bump
Grid
Miscellaneous
Detail
Speed
Click to select single object. Shift+Click to de/select multiple objects.
14.45900, 360.46400
In Memory

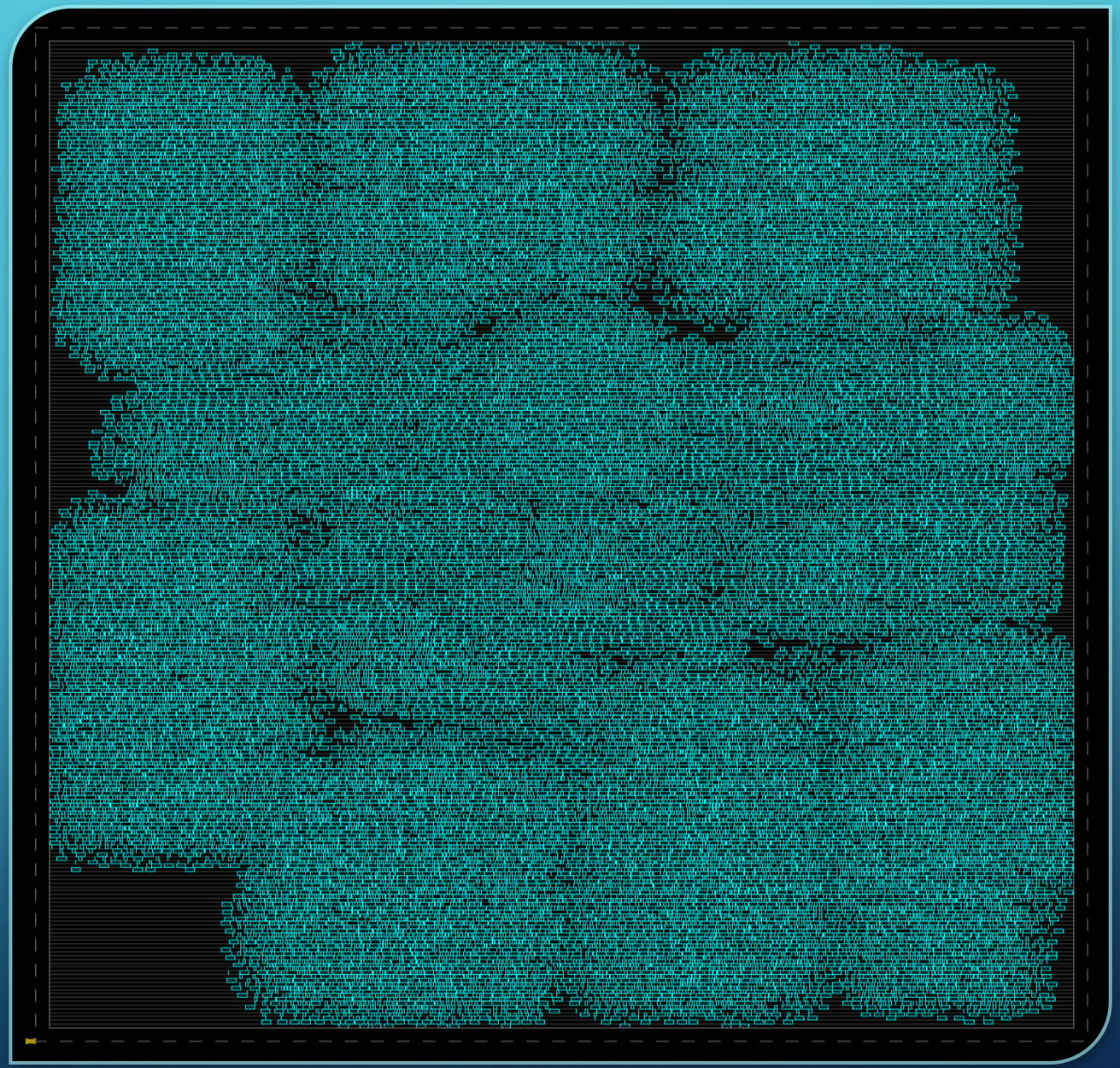
```
arting congestion repair ...
[NR-eGR] honorMsvRouteConstraint: false
[NR-eGR] honorClockSpecNDR      : 0
[NR-eGR] minRouteLayer          : 2
[NR-eGR] maxRouteLayer          : 127
[NR-eGR] numTracksPerClockWire  : 0
[NR-eGR] Layer1 has no routable track
[NR-eGR] Layer2 has single uniform track structure
[NR-eGR] Layer3 has single uniform track structure
[NR-eGR] Layer4 has single uniform track structure
[NR-eGR] Layer5 has single uniform track structure
[NR-eGR] Layer6 has single uniform track structure
[NR-eGR] Layer7 has single uniform track structure
[NR-eGR] Layer8 has single uniform track structure
[NR-eGR] Layer9 has single uniform track structure
[NR-eGR] Layer10 has single uniform track structure
[NR-eGR] numRoutingBlks=0 numInstBlks=0 numPGBlocks=532 numBumpBlks=0 numBoundaryFakeBlks=0
[NR-eGR] numPreroutedNet = 0  numPreroutedWires = 0
[NR-eGR] Read numTotalNets=40162  numIgnoredNets=0
[NR-eGR] There are 1 clock nets ( 0 with NDR ).
[NR-eGR] ============ Routing rule table ============
[NR-eGR] Rule id 0. Nets 40162
[NR-eGR] id=0  ndrTrackId=0  ndrViaId=-1  extraSpace=0  numShields=0  maxHorDemand=1  maxVerDemand=1
[NR-eGR] Pitch:  L1=270  L2=280  L3=280  L4=560  L5=560  L6=560  L7=1680  L8=1680  L9=3200  L10=3360
[NR-eGR] ======================================
[NR-eGR]
[NR-eGR] Layer group 1: route 40162 net(s) in layer range [2, 10]
[NR-eGR] earlyGlobalRoute overflow of layer group 1: 0.00% H + 0.00% V. EstWL: 5.102762e+05um
[NR-eGR]
[NR-eGR] Overflow after earlyGlobalRoute (GR compatible) 0.00% H + 0.00% V
[NR-eGR] Overflow after earlyGlobalRoute 0.00% H + 0.00% V
Local HotSpot Analysis: normalized max congestion hotspot area = 0.00, normalized total congestion hots
0.00 (area is in unit of 4 std-cell row bins)
Skipped repairing congestion.
[NR-eGR] ------------------------------------------------------------------------
[NR-eGR] Layer1(metal1)(F) length: 0.000000e+00um, number of vias: 138869
[NR-eGR] Layer2(metal2)(V) length: 2.347267e+05um, number of vias: 207680
[NR-eGR] Layer3(metal3)(H) length: 2.413505e+05um, number of vias: 5787
[NR-eGR] Layer4(metal4)(V) length: 4.230372e+04um, number of vias: 1021
[NR-eGR] Layer5(metal5)(H) length: 1.185954e+04um, number of vias: 324
[NR-eGR] Layer6(metal6)(V) length: 6.028169e+03um, number of vias: 20
[NR-eGR] Layer7(metal7)(H) length: 2.682400e+02um, number of vias: 3
[NR-eGR] Layer8(metal8)(V) length: 1.295000e+01um, number of vias: 0
[NR-eGR] Layer9(metal9)(H) length: 0.000000e+00um, number of vias: 0
[NR-eGR] Layer10(metal10)(V) length: 0.000000e+00um, number of vias: 0
[NR-eGR] Total length: 5.365497e+05um, number of vias: 353704
[NR-eGR] ------------------------------------------------------------------------
[NR-eGR] Total clock nets wire length: 3.342357e+04um
[NR-eGR] ------------------------------------------------------------------------
End of congRepair (cpu=0:00:01.5, real=0:00:01.0)
*** Finishing placeDesign default flow ***
***** Total cpu  0:2:22
***** Total real time  0:1:4
**placeDesign ... cpu = 0: 2:22, real = 0: 1: 4, mem = 1719.2M **

*** Summary of all messages that are not suppressed in this session:
Severity  ID               Count  Summary
WARNING   IMPDC-1629           1  The default delay limit was set to %d. T...
WARNING   IMPSP-9025           1  No scan chain specified/traced.
*** Message Summary: 2 warning(s), 0 error(s)
```



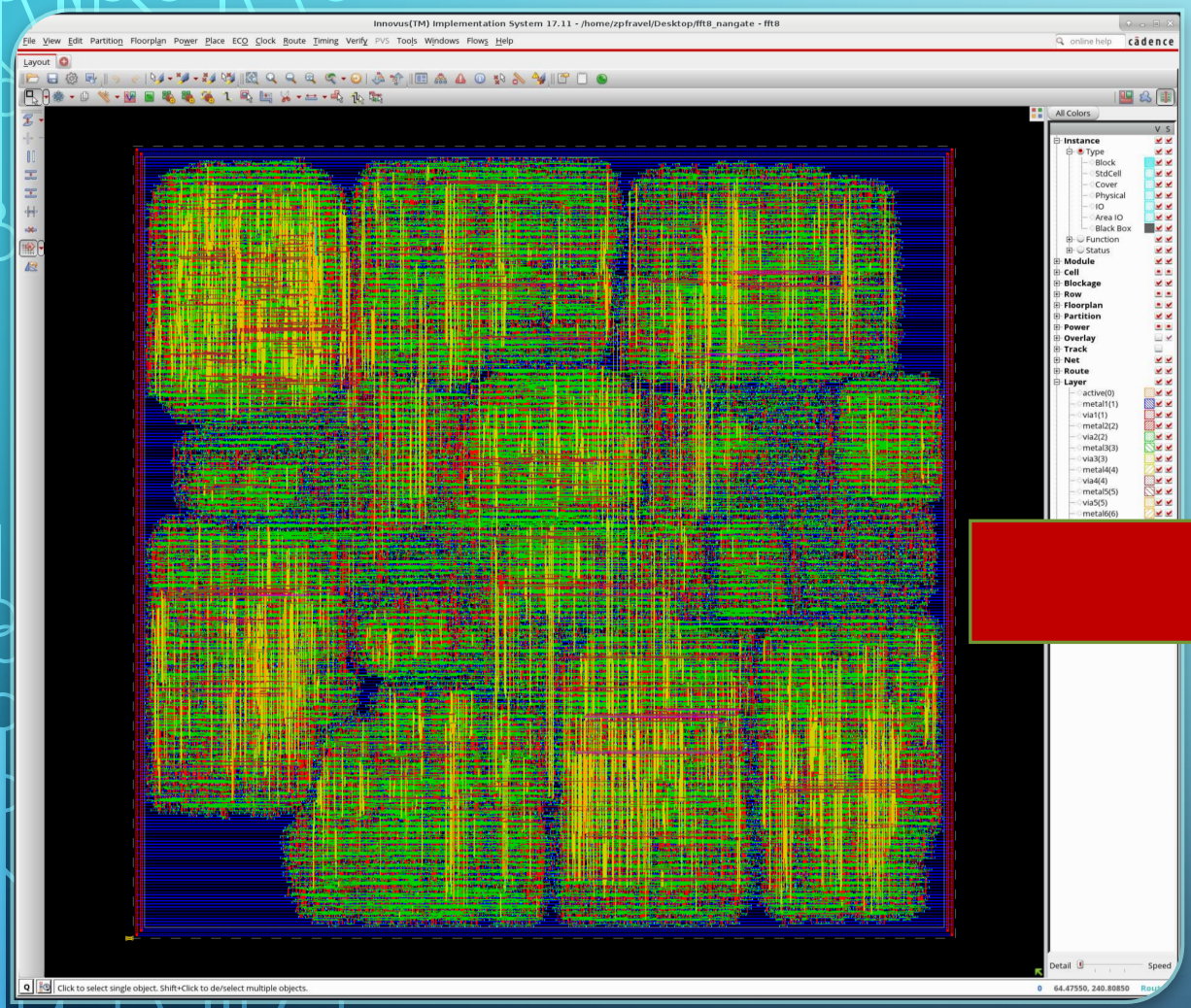


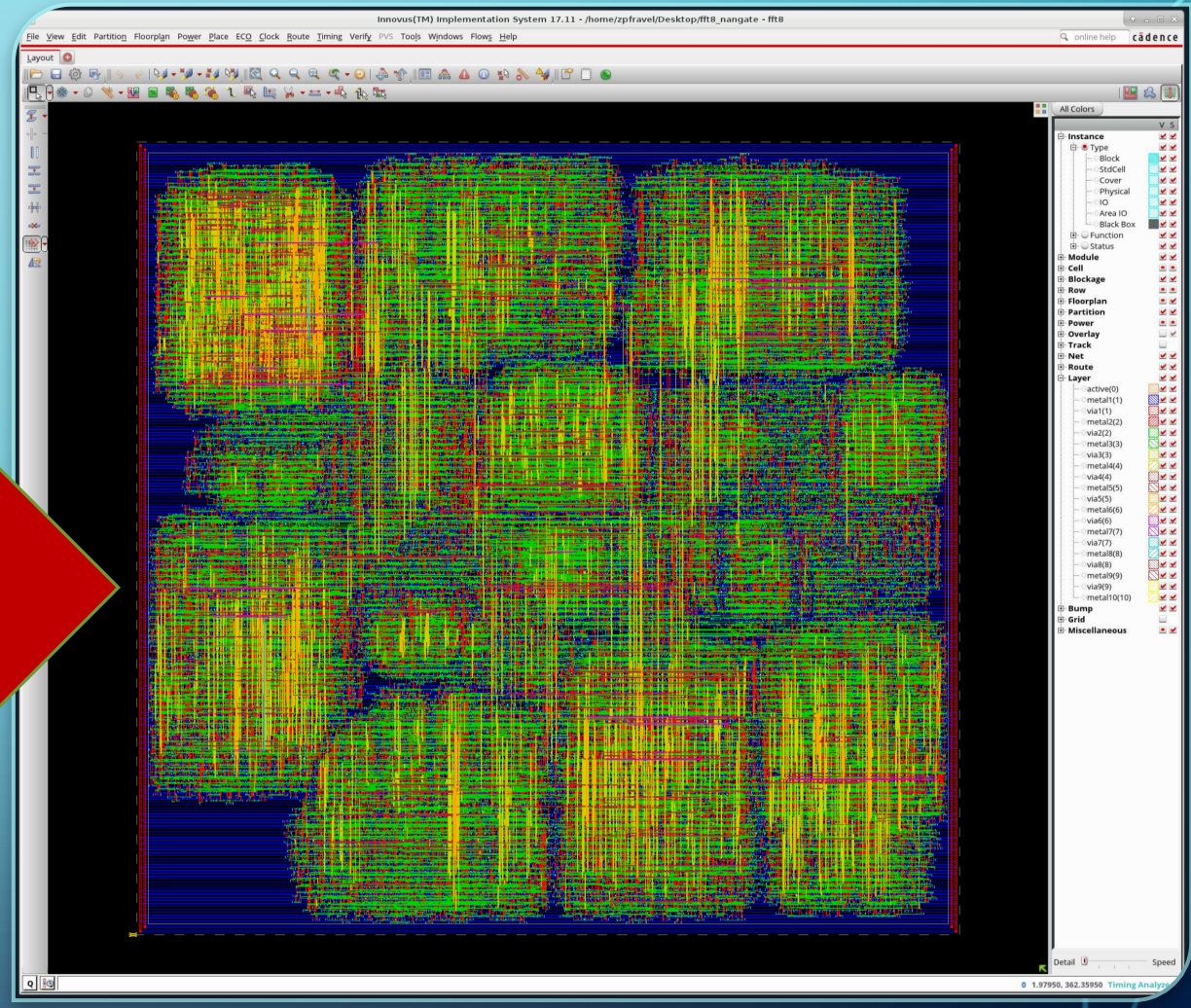
PLACEMENT

STANDARD CELLS



PRE-CTS OPTIMIZATION



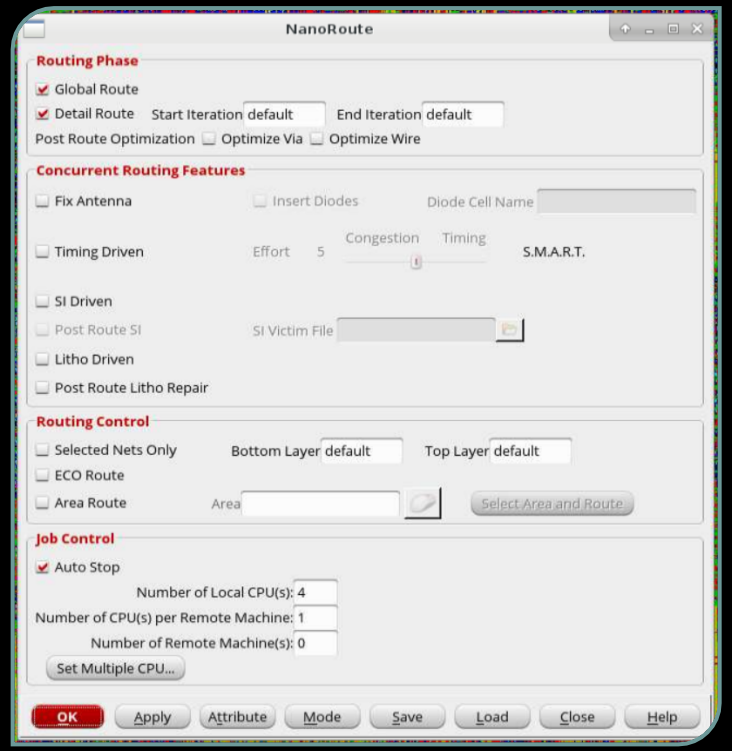


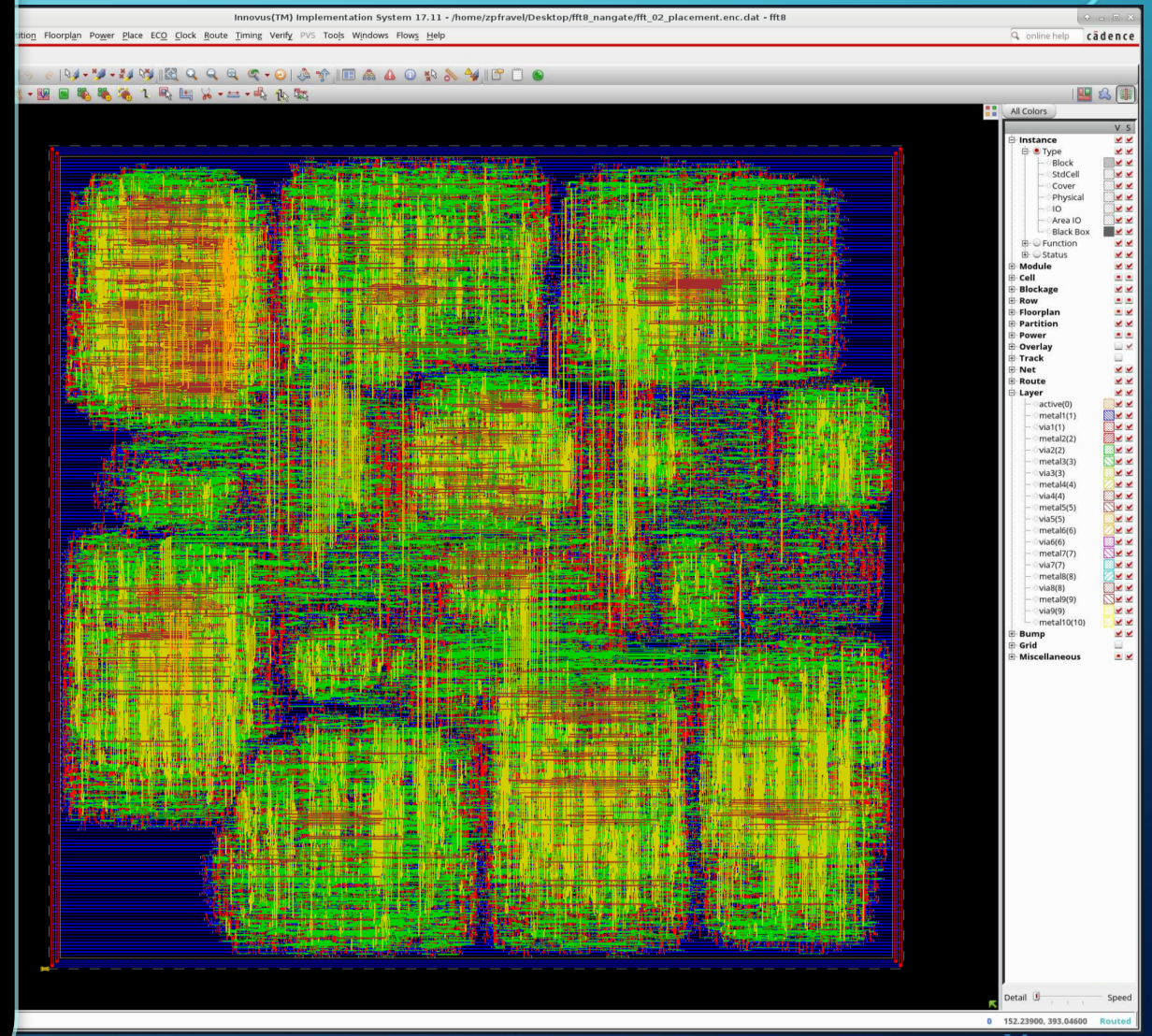
PRE-CTS OPTIMIZATION SUMMARY

```
------------------------------------------------------------
     optDesign Final Summary
------------------------------------------------------------

Setup views included:
 NG_view_typ

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):| 38.576  | 38.576  | 39.380  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|  10749  |  10749  |  3714   |
+--------------------+---------+---------+---------+

+----------------+--------------------------------+------------------+
|                |              Real              |       Total      |
|    DRVs        +------------------+-------------+------------------|
|                |  Nr nets(terms)  | Worst Vio   |  Nr nets(terms)  |
+----------------+------------------+-------------+------------------+
|   max_cap      |      0 (0)       |   0.000     |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000     |      0 (0)       |
|   max_fanout   |      0 (0)       |     0       |      0 (0)       |
|   max_length   |      0 (0)       |     0       |      0 (0)       |
+----------------+------------------+-------------+------------------+

Density: 60.313%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
**optDesign ... cpu = 0:04:19, real = 0:01:53, mem = 1599.0M, totSessionCpu=0:09:45 **
*** Finished optDesign ***
innovus 7>
```

ROUTING

```
tart DRC checking..
#   number of violations = 0
#cpu time = 00:00:25, elapsed time = 00:00:06, memory = 1589.91 (MB), peak = 1652.30 (MB)
#CELL_VIEW fft8,init has no DRC violation.
#Total number of DRC violations = 0
#   number of violations = 0
#cpu time = 00:00:31, elapsed time = 00:00:10, memory = 1439.07 (MB), peak = 1652.30 (MB)
#CELL_VIEW fft8,init has no DRC violation.
#Total number of DRC violations = 0
#Post Route wire spread is done.
#Total wire length = 543156 um.
#Total half perimeter of net bounding box = 414969 um.
#Total wire length on LAYER metal1 = 21898 um.
#Total wire length on LAYER metal2 = 200728 um.
#Total wire length on LAYER metal3 = 219580 um.
#Total wire length on LAYER metal4 = 78706 um.
#Total wire length on LAYER metal5 = 19888 um.
#Total wire length on LAYER metal6 = 2356 um.
#Total wire length on LAYER metal7 = 0 um.
#Total wire length on LAYER metal8 = 0 um.
#Total wire length on LAYER metal9 = 0 um.
#Total wire length on LAYER metal10 = 0 um.
#Total number of vias = 272614
#Up-Via Summary (total 272614):
#
#---------------------
# metal1         140665
# metal2         115041
# metal3          14995
# metal4           1703
# metal5            210
#---------------------
#                272614
#
#detailRoute Statistics:
#Cpu time = 00:01:01
#Elapsed time = 00:00:19
#Increased memory = 4.45 (MB)
#Total memory = 1436.95 (MB)
#Peak memory = 1652.30 (MB)
#
#globalDetailRoute statistics:
#Cpu time = 00:01:10
#Elapsed time = 00:00:26
#Increased memory = 9.20 (MB)
#Total memory = 1396.46 (MB)
#Peak memory = 1652.30 (MB)
#Number of warnings = 24
#Total number of warnings = 110
#Number of fails = 0
#Total number of fails = 0
#Complete globalDetailRoute on Mon Dec  4 01:17:43 2017
#
#routeDesign: cpu time = 00:01:11, elapsed time = 00:00:26, memory = 1396.46 (MB), peak = 1652.30 (MB)

*** Summary of all messages that are not suppressed in this session:
Severity  ID               Count  Summary
WARNING   IMPCK-8086           1  The command %s is obsolete and will be r...
*** Message Summary: 1 warning(s), 0 error(s)
```

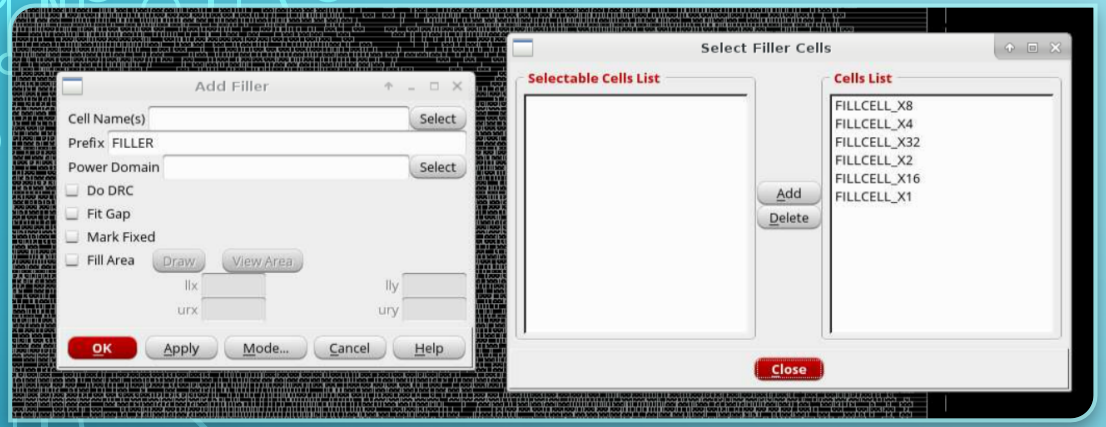




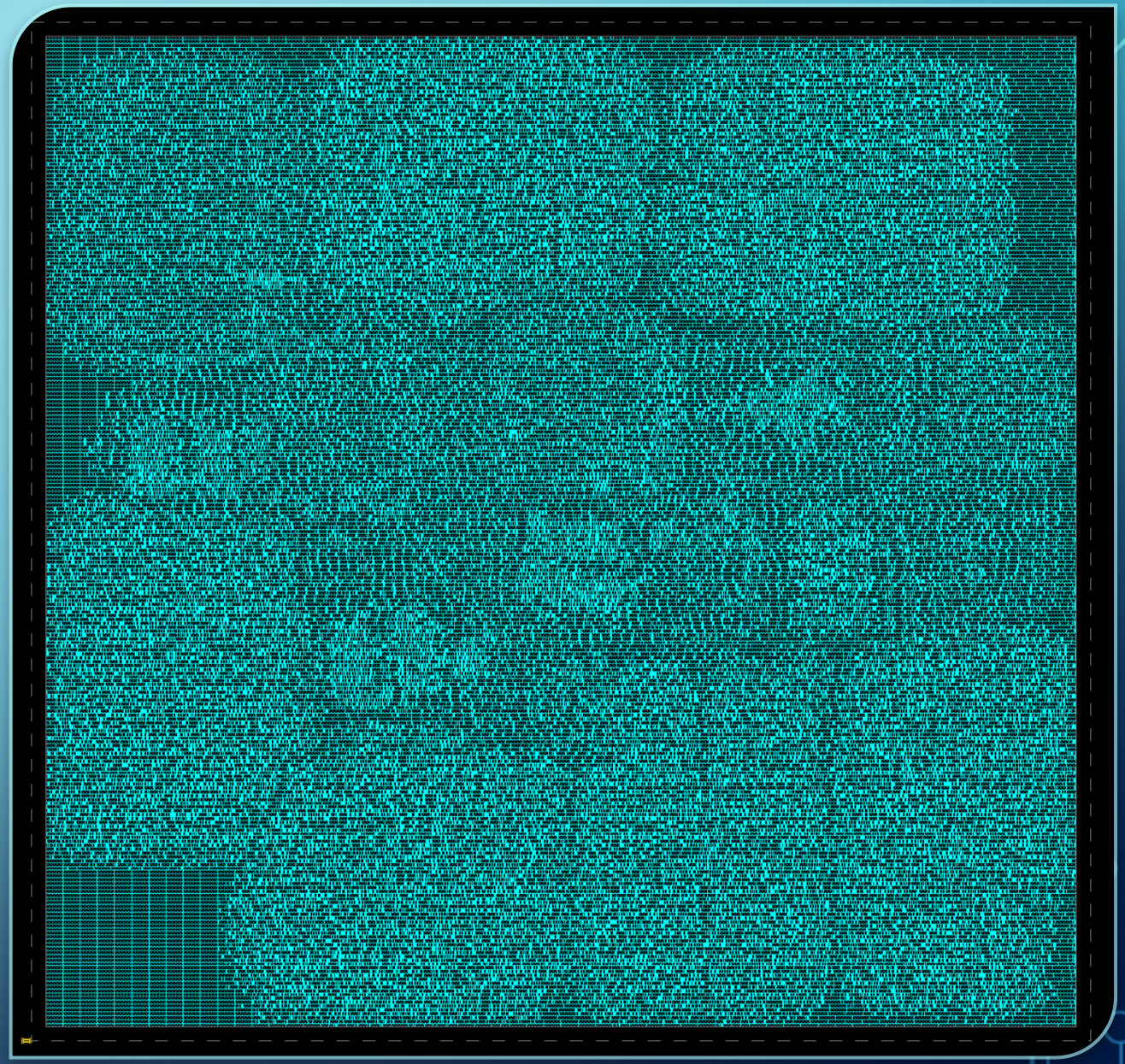
POST ROUTE OPTIMIZATION SUMMARY

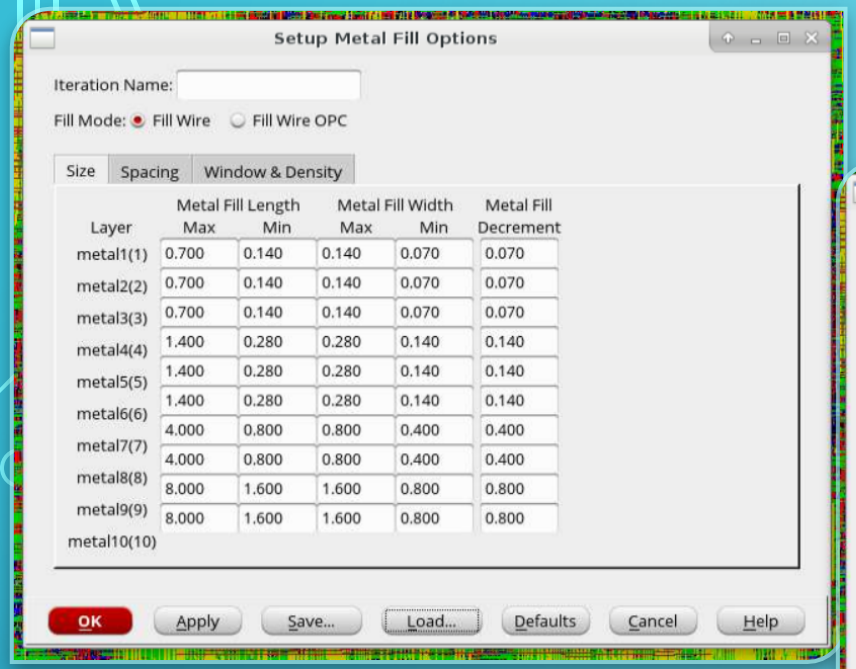
```
------------------------------------------------------------
     optDesign Final SI Timing Summary
------------------------------------------------------------

Setup views included:
 NG_view_typ

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):| 38.587  | 38.587  | 39.200  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|  10749  |  10749  |  3714   |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 60.314%
Total number of glitch violations: 0
------------------------------------------------------------
**optDesign ... cpu = 0:01:42, real = 0:00:59, mem = 1644.4M, totSessionCpu=0:16:48 **
 ReSet Options after AAE Based Opt flow
Opt: RC extraction mode changed to 'detail'
**WARN: (IMPOPT-3195):  Analysis mode has changed.
Type 'man IMPOPT-3195' for more detail.
*** Finished optDesign ***
Info: Destroy the CCOpt slew target map.
```

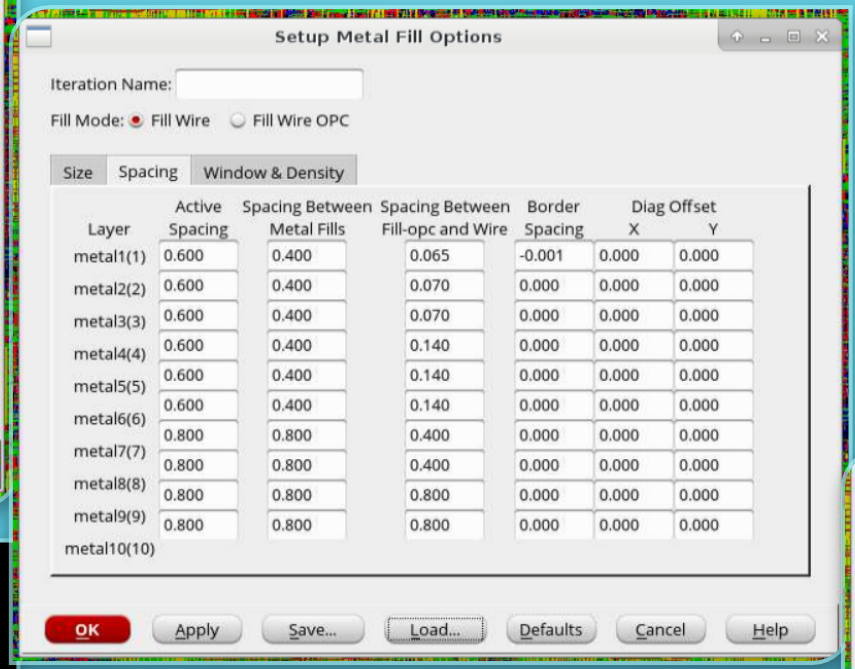
FILLER CELL SUMMARY

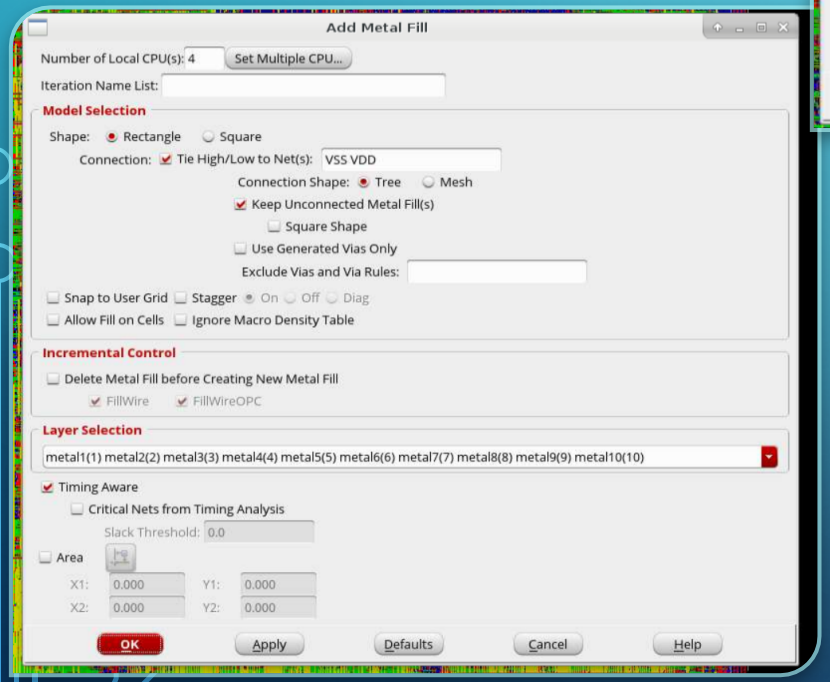



```
*INFO: Adding fillers to top-module.
*INFO:    Added 1254 filler insts (cell FILLCELL_X32 / prefix FILLER).
*INFO:    Added 1124 filler insts (cell FILLCELL_X16 / prefix FILLER).
*INFO:    Added 4281 filler insts (cell FILLCELL_X8 / prefix FILLER).
*INFO:    Added 13327 filler insts (cell FILLCELL_X4 / prefix FILLER).
*INFO:    Added 51683 filler insts (cell FILLCELL_X1 / prefix FILLER).
*INFO:    Added 0 filler inst  (cell FILLCELL_X2 / prefix FILLER).
*INFO: Total 71669 filler insts added - prefix FILLER (CPU: 0:00:03.5).
For 71669 new insts, *** Applied 0 GNC rules (cpu = 0:00:00.0)
innovus 1>
```

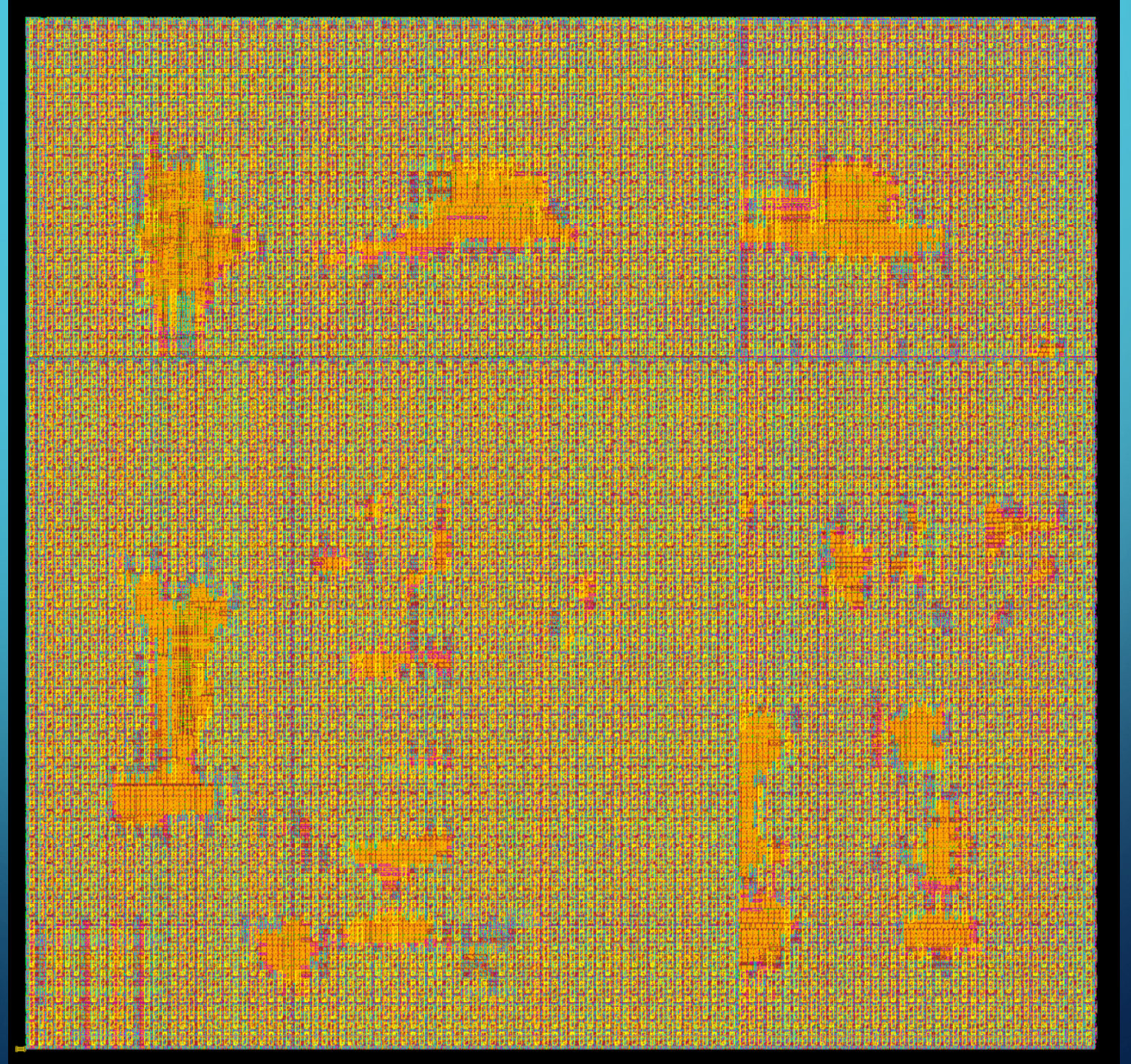


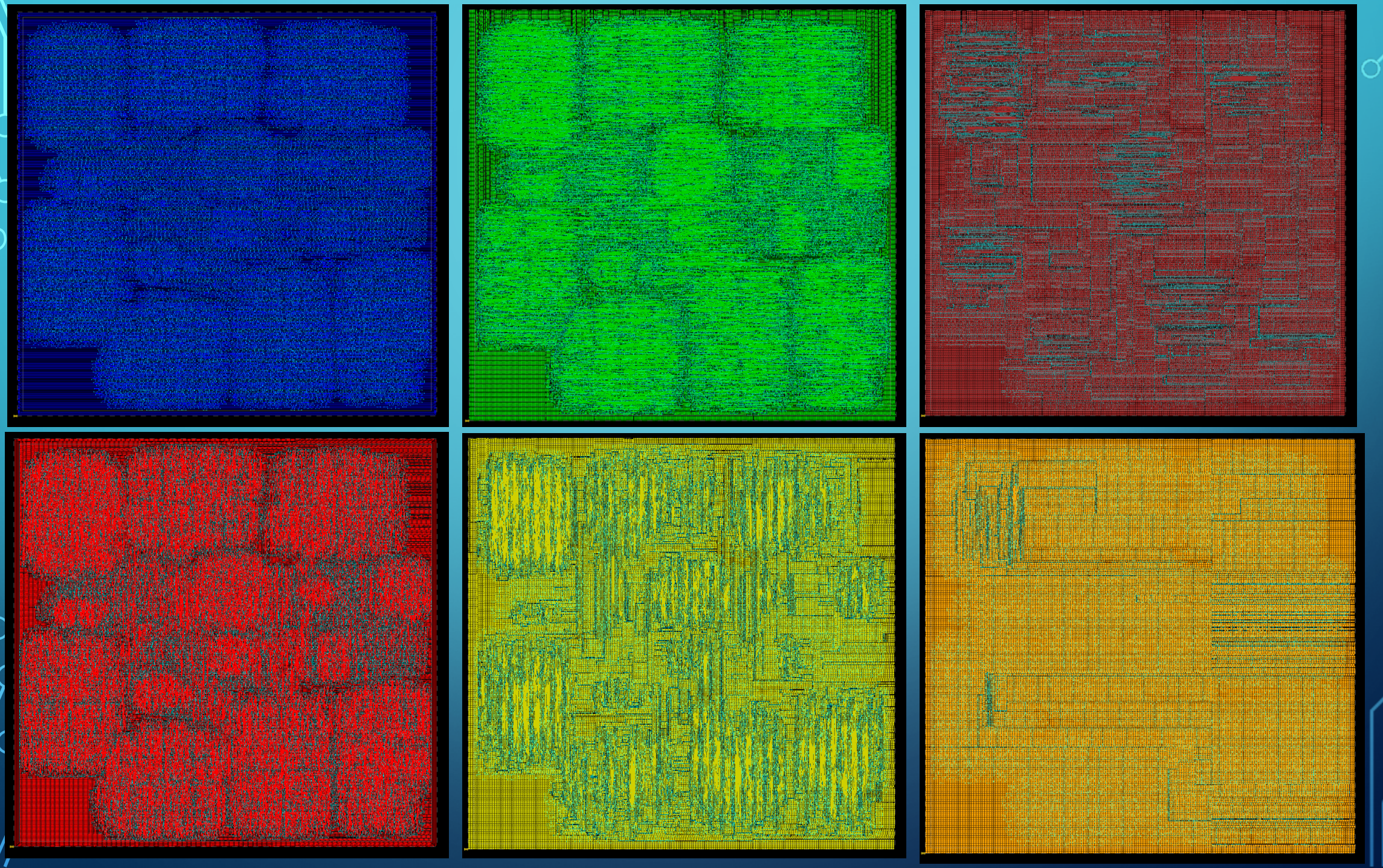


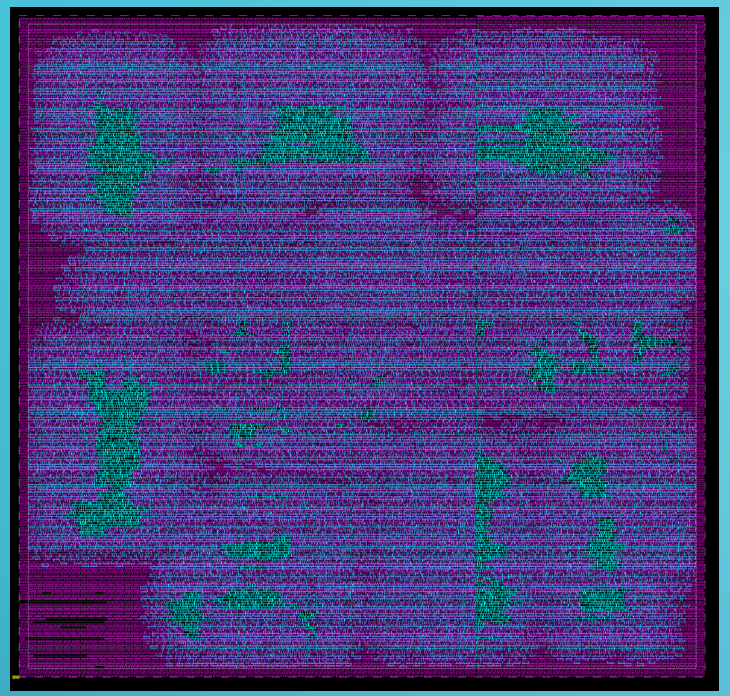


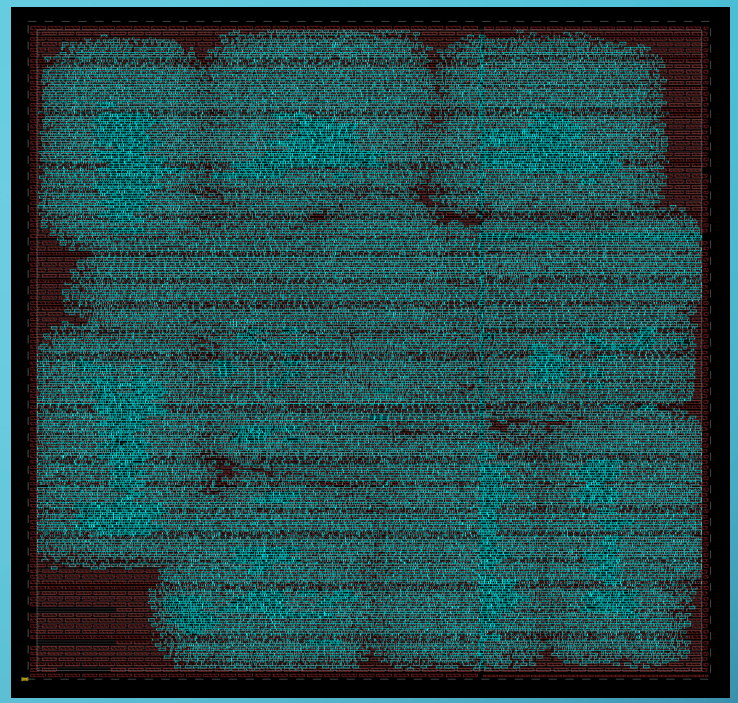


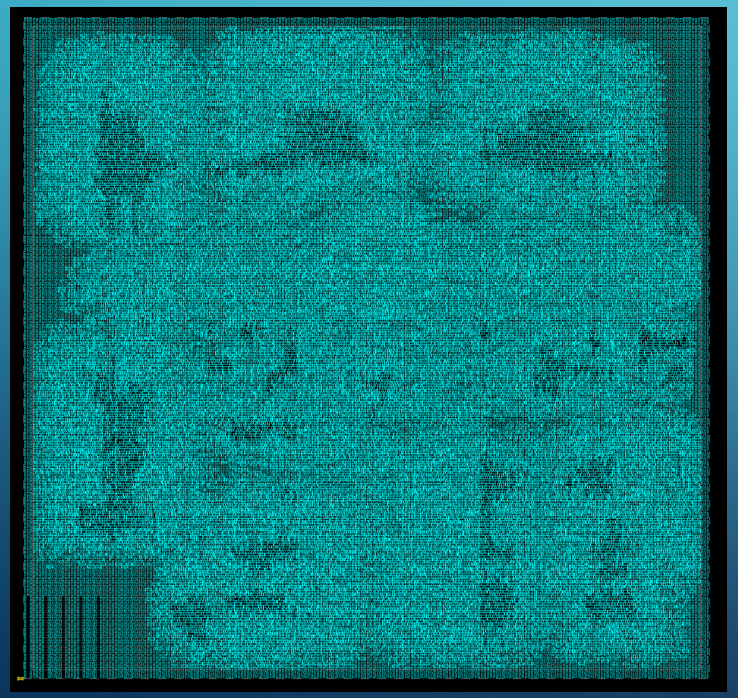
METAL FILL SETTINGS

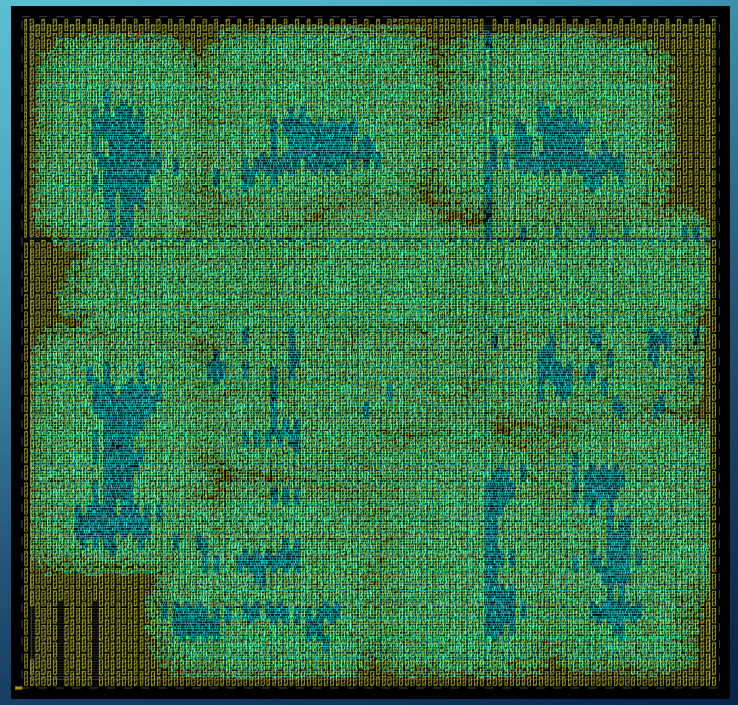


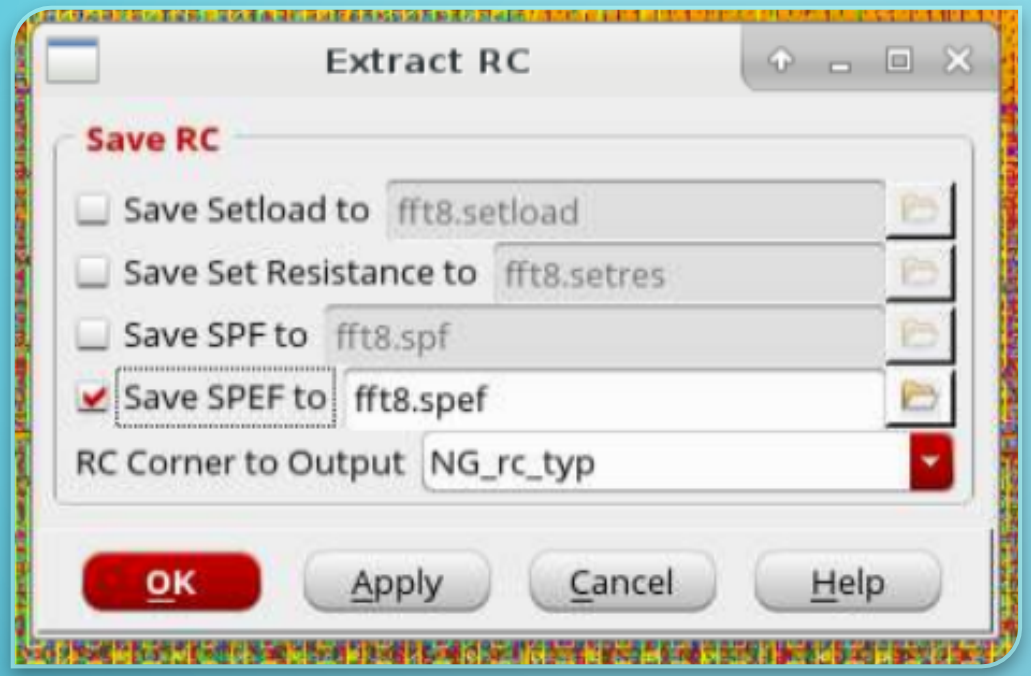






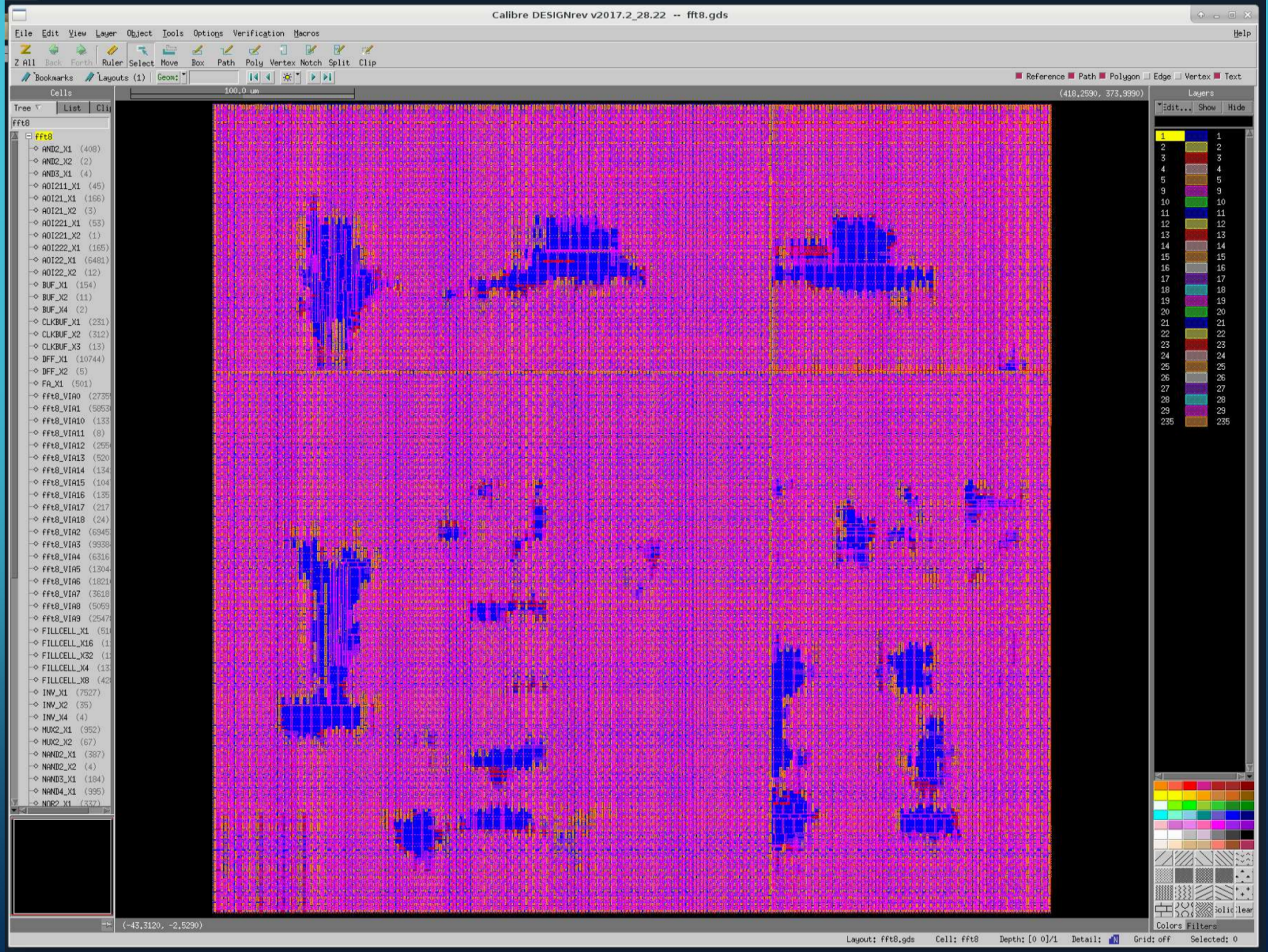


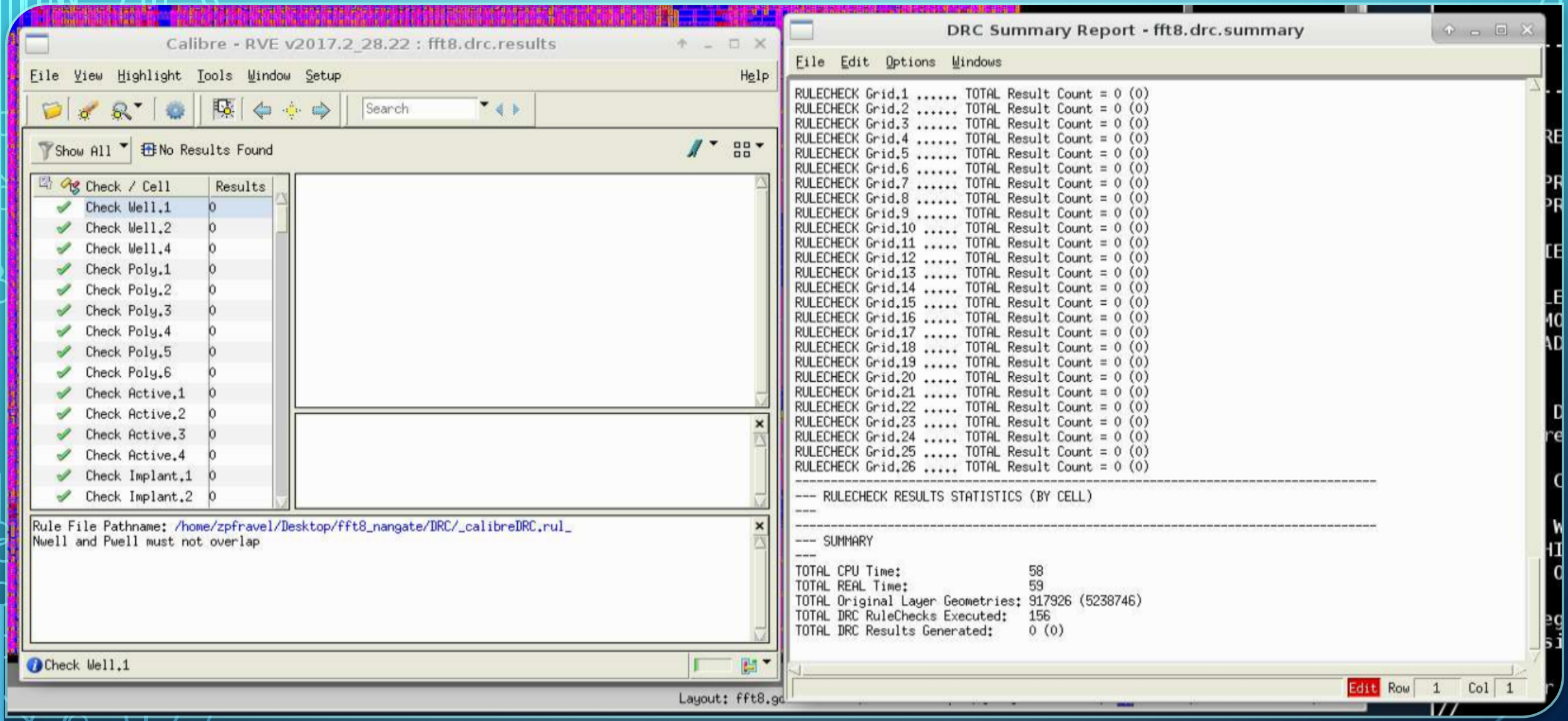




RC EXTRACTION

```
Number of Extracted Resistors     : 760633
Number of Extracted Ground Cap.   : 799593
Number of Extracted Coupling Cap. : 1236564
Filtering XCap in 'relativeOnly' mode using values relative_c_threshold=0.03 and total_c_threshold=5fF.
 Corner: NG_rc_typ
Checking LVS Completed (CPU Time= 0:00:00.1  MEM= 1654.1M)
PostRoute (effortLevel low) RC Extraction DONE (CPU Time: 0:00:06.5  Real Time: 0:00:07.0  MEM: 1654.137M)
RC Out has the following PVT Info:
   RC:NG_rc_typ, Operating temperature 25 C
Dumping Spef file.....
Printing D_NET...
rcOut completed:: 100 %
RC Out from RCDB Completed (CPU Time= 0:00:01.5  MEM= 1654.1M)
```


Calibre DESIGNrev v2017.2_28.22 -- fft8.gds
File Edit View Layer Object Tools Options Verification Macros Help
Z All Back Forth Ruler Select Move Box Path Poly Vertex Notch Split Clip
Bookmarks Layouts (1) Geom:
Reference Path Polygon Edge Vertex Text
Cells
Tree List
fft8
AND2_X1 (408)
AND2_X2 (2)
AND3_X1 (4)
AOI211_X1 (45)
AOI21_X1 (166)
AOI21_X2 (3)
AOI221_X1 (53)
AOI221_X2 (1)
AOI222_X1 (165)
AOI22_X1 (6481)
AOI22_X2 (12)
BUF_X1 (154)
BUF_X2 (11)
BUF_X4 (2)
CLKBUF_X1 (231)
CLKBUF_X2 (312)
CLKBUF_X3 (13)
DFF_X1 (10744)
DFF_X2 (5)
FA_X1 (501)
INV_X1 (7527)
INV_X2 (35)
INV_X4 (4)
MUX2_X1 (952)
MUX2_X2 (67)
NAND2_X1 (387)
NAND2_X2 (4)
NAND3_X1 (184)
NAND4_X1 (995)
100.0 um
(418,2590, 373,9990)
Layers
Edit... Show Hide
Colors Filters
(-43,3120, -2,5290)
Layout: fft8.gds Cell: fft8 Depth: [0 0]/1 Detail: Grid: off Selected: 0



DRC REPORT

CALIBRE READS .GDS LAYOUT FILE EXPORTED FROM INNOVUS

TIMING AND POWER ANALYSIS (POST ROUTE)

- Static Timing Analysis (STA) with Synopsys Primetime

- 40ns clock period
- 25 MHz
- Uses Parasitic information generated by Innovus .spef file
- 0.5 switching probability

```
suppress_message "RC-004 RC-008 RC-009 PTE-060"

set target_library "lib/db/NangateOpenCellLibrary_typical_ecsm.db"
set link_library "* lib/db/NangateOpenCellLibrary_typical_ecsm.db"

set topname fft8

set myPeriod_ns 40
set myClk clk

read_verilog fft8_routed.v

current_design $topname

link

create_clock -period $myPeriod_ns $myClk

set_ideal_network [get_port $myClk]

read_parasitics $topname.spef -keep_capacitive_coupling

complete_net_parasitics -complete_with zero
report_annotated_parasitics -check

set power_enable_analysis TRUE

set_switching_activity -static_probability 0.5 -toggle_rate 0.15 -base_clock $myClk [remove_from_collection [all_inputs] $myClk]
set_switching_activity -static_probability 0.5 -toggle_rate 0.15 -base_clock $myClk -type registers -hierarchy

update_timing
report_timing -group $myClk -capacitance -transition_time  > $topname.timing.pt.rpt

update_power
report_power >> $topname.power.pt.rpt

exit
```

PRIMETIME SCRIPT

```
****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
        -group clk
        -transition_time
        -capacitance
        -sort_by slack
Design : fft8
Version: M-2017.06-SP1
Date   : Mon Dec  4 02:21:46 2017
****************************************


  Startpoint: stage9/codeBlockIsnt16714/tm41_reg[1]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: stage9/codeBlockIsnt16714/m14983/q_reg[0][15]
              (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                     Cap      Trans       Incr       Path
  -----------------------------------------------------------------------------
  clock clk (rise edge)                                0.00       0.00       0.00
  clock network delay (ideal)                                     0.00       0.00
  stage9/codeBlockIsnt16714/tm41_reg[1]/CK (DFF_X1)
                                                       0.00       0.00       0.00 r
  stage9/codeBlockIsnt16714/tm41_reg[1]/QN (DFF_X1)
                                           36.98       0.09       0.15 &     0.15 r
  U11050/ZN (NAND2_X1)                      3.32       0.02       0.03 &     0.18 f
  U11051/ZN (OAI21_X1)                     17.48       0.09       0.06 &     0.24 r
  U11052/ZN (INV_X1)                       24.70       0.04       0.07 &     0.31 f
  U11056/ZN (AOI21_X1)                     18.91       0.10       0.14 &     0.45 r
  U11087/ZN (INV_X1)                       10.18       0.03       0.04 &     0.49 f
  U11088/ZN (OAI22_X1)                      4.54       0.04       0.06 &     0.55 r
  U11089/Z (XOR2_X1)                        5.35       0.04       0.07 &     0.62 r
  U11090/ZN (OAI22_X1)                      1.74       0.01       0.03 &     0.65 f
  U11091/ZN (AOI21_X1)                      3.70       0.03       0.05 &     0.70 r
  U11092/ZN (AOI21_X1)                      1.71       0.01       0.02 &     0.72 f
  U11098/ZN (OAI21_X1)                      3.94       0.03       0.04 &     0.76 r
  U11103/ZN (AOI222_X1)                     4.01       0.02       0.03 &     0.79 f
  intadd_1/U8/CO (FA_X1)                    2.84       0.01       0.08 &     0.87 f
  intadd_1/U7/CO (FA_X1)                    3.01       0.01       0.07 &     0.94 f
  intadd_1/U6/CO (FA_X1)                    2.93       0.01       0.07 &     1.02 f
  intadd_1/U5/CO (FA_X1)                    2.91       0.01       0.07 &     1.09 f
  intadd_1/U4/CO (FA_X1)                    2.91       0.01       0.07 &     1.16 f
  intadd_1/U3/CO (FA_X1)                    3.19       0.02       0.07 &     1.23 f
  intadd_1/U2/CO (FA_X1)                    3.34       0.02       0.07 &     1.31 f
  U11166/ZN (OAI21_X1)                      1.94       0.02       0.04 &     1.34 r
  U11167/ZN (OAI21_X1)                      1.21       0.01       0.02 &     1.36 f
  stage9/codeBlockIsnt16714/m14983/q_reg[0][15]/D (DFF_X1)
                                                       0.01       0.00 &     1.36 f
  data arrival time                                                           1.36

  clock clk (rise edge)                                0.00      40.00      40.00
  clock network delay (ideal)                                     0.00      40.00
  clock reconvergence pessimism                                   0.00      40.00
  stage9/codeBlockIsnt16714/m14983/q_reg[0][15]/CK (DFF_X1)                 40.00 r
  library setup time                                             -0.04      39.96
  data required time                                                        39.96
  -----------------------------------------------------------------------------
  data required time                                                        39.96
  data arrival time                                                         -1.36
  -----------------------------------------------------------------------------
  slack (MET)                                                               38.60


1
```

PRIMETIME TIMING ANALYSIS

```
****************************************
Report : Averaged Power
Design : fft8
Version: M-2017.06-SP1
Date   : Mon Dec  4 02:22:01 2017
****************************************



  Attributes
  ----------
      i  -  Including register clock pin internal power
      u  -  User defined power group

                          Internal  Switching  Leakage    Total
Power Group               Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
clock_network             9.744e-04    0.0000    0.0000 9.744e-04 (27.29%)  i
register                  3.844e-04 1.092e-04 8.498e-04 1.343e-03 (37.62%)
combinational             2.362e-04 2.632e-04 7.536e-04 1.253e-03 (35.09%)
sequential                   0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                       0.0000    0.0000    0.0000    0.0000 ( 0.00%)
io_pad                       0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                    0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 3.724e-04   (10.43%)
  Cell Internal Power  = 1.595e-03   (44.67%)
  Cell Leakage Power   = 1.603e-03   (44.90%)
                         ---------
Total Power            = 3.571e-03  (100.00%)

1
```

PRIMETIME POWER ANALYSIS

DESIGN SUMMARY REPORTS

General Design Information

Design Status	Routed
Design Name	fft8
# Instances	109414
# Hard Macros	0
# Std Cells	109414
# Pads	0
# Net	40536
# Special Net	3
# IO Pins	68
# Pins	139242
# PG Pins	218828
Average Pins Per Net(Signal)	3.435

General Library Information

# Routing Layers	10
# Masterslice Layers	2
# Pin Layers	2
# Layers	22
# Pins without Physical Port	0
# Pins in Library without Timing Lib	0
# Pins Missing Direction	0
Antenna Summary Report	For more information click here
# Cells Missing LEF Info	0
# Cells with Dimension Errors	0

STANDARD CELL SUMMARY

AND2_X1	408	434.1120
AND2_X2	2	2.6600
AND3_X1	4	5.3200
AOI211_X1	45	59.8500
AOI21_X1	166	176.6240
AOI21_X2	3	5.5860
AOI221_X1	53	84.5880
AOI221_X2	1	2.9260
AOI222_X1	165	351.1200
AOI22_X1	6481	8619.7300
AOI22_X2	12	28.7280
BUF_X1	154	122.8920
BUF_X2	11	11.7040
BUF_X4	2	3.7240
CLKBUF_X1	231	184.3380
CLKBUF_X2	312	331.9680
CLKBUF_X3	13	17.2900
DFF_X1	10744	48584.3680
DFF_X2	5	25.2700
FA_X1	501	2132.2560
FILLCELL_X1	51683	13747.6780
FILLCELL_X16	1124	4783.7440
FILLCELL_X32	1254	10674.0480
FILLCELL_X4	13327	14179.9280
FILLCELL_X8	4281	9109.9680

INV_X1	7527	4004.3640
INV_X2	35	27.9300
INV_X4	4	5.3200
MUX2_X1	952	1772.6240
MUX2_X2	67	160.3980
NAND2_X1	387	308.8260
NAND2_X2	4	5.3200
NAND3_X1	184	195.7760
NAND4_X1	995	1323.3500
NOR2_X1	337	268.9260
NOR2_X2	615	817.9500
NOR3_X1	26	27.6640
NOR4_X1	197	262.0100
OAI211_X1	34	45.2200
OAI21_X1	251	267.0640
OAI221_X1	53	84.5880
OAI222_X1	1	2.1280
OAI22_X1	6486	8626.3800
OR2_X1	83	88.3120
OR2_X2	46	61.1800
OR3_X1	1	1.3300
OR3_X2	4	6.3840
OR4_X1	33	52.6680
XNOR2_X1	60	95.7600
XOR2_X1	44	70.2240
XOR2_X2	6	14.3640

DESIGN SUMMARY REPORTS

Floorplan/Placement Information

Total area of Standard cells	132276.480 um^2
Total area of Standard cells(Subtracting Physical Cells)	79781.114 um^2
Total area of Macros	0.000 um^2
Total area of Blockages	0.000 um^2
Total area of Pad cells	0.000 um^2
Total area of Core	132290.984 um^2
Total area of Chip	139725.186 um^2
Effective Utilization	1.0000e+00
Number of Cell Rows	259
% Pure Gate Density #1 (Subtracting BLOCKAGES)	99.989%
% Pure Gate Density #2 (Subtracting BLOCKAGES and Physical Cells)	60.307%
% Pure Gate Density #3 (Subtracting MACROS)	99.989%
% Pure Gate Density #4 (Subtracting MACROS and Physical Cells)	60.307%
% Pure Gate Density #5 (Subtracting MACROS and BLOCKAGES)	99.989%
% Pure Gate Density #6 (Subtracting MACROS and BLOCKAGES for insts are not placed)	60.307%
% Core Density (Counting Std Cells and MACROs)	99.989%
% Core Density #2(Subtracting Physical Cells)	60.307%
% Chip Density (Counting Std Cells and MACROs and IOs)	94.669%
% Chip Density #2(Subtracting Physical Cells)	57.099%
# Macros within 5 sites of IO pad	No
Macro halo defined?	No

Wire Length Distribution

Total metal1 wire length	21895.9200 um
Total metal2 wire length	200726.7100 um
Total metal3 wire length	219582.3700 um
Total metal4 wire length	78705.9000 um
Total metal5 wire length	19887.8400 um
Total metal6 wire length	2355.9200 um
Total metal7 wire length	0.0000 um
Total metal8 wire length	0.0000 um
Total metal9 wire length	0.0000 um
Total metal10 wire length	0.0000 um
Total wire length	543154.6600 um
Average wire length/net	13.3993 um
Area of Power Net Distribution	For more information click here